REMARKS

Upon entry of this amendment, claims 1, 5, 6, 8, 11-24, and 31-33 will be pending in the application. By this amendment, claim 1 is amended and claims 25-30 are canceled without prejudice or disclaimer. The above amendments do not add new matter to the application and are fully supported by the original disclosure. For example, support for the amendments is provided in the claims as originally filed. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Amendment is Proper for Entry

Applicants submit that the instant amendment is proper for entry because all of the presented claims are in condition for allowance, as explained in detail below, and the amendments to the claims do not raise new issues that would require further search and/or consideration. More specifically, claim 1 is amended solely to address a grammatical objection that was raised by the Examiner. Furthermore, claim 1 is amended using the wording suggested by the Examiner in the Final Office Action. Accordingly, Applicants submit the Examiner has considered the language of amended claim 1, such that the amendment does not raise new issues that would require further search and/or consideration. Moreover, the cancellation of claims 25-30 does not raise new issues that would require further search and/or consideration.

Alternatively, Applicants submit that entry of the instant amendment is proper because the amendment places the application in better form for appeal.

Allowable Claims

Applicants appreciate the indication that claims 6, 8, 14, 15, 17, 21, 22, 24, 29, and 30 contain allowable subject matter. However, these claims are not presented in independent form at this time, as Applicants submit that all of the claims are in condition for allowance for the following reasons.

Objection to Claims

Claim 1 is objected to for grammatical reasons. By this response, claim 1 is amended pursuant to the Examiner's suggestion. Accordingly, Applicants submit the objection is moot, and respectfully request the objection to claim 1 be withdrawn.

35 U.S.C. §102 Rejection

Claims 1, 5, 11-13, 16, 18-20, 23, 25-28, and 31-33 are rejected under 35 U.S.C. §102(b) as being anticipated by the article entitled "Post-route optimization for improved yield using a rubber-band wiring model" by SU et al. (1997) (hereafter referred to as "SU"). This rejection is respectfully traversed.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See MPEP §2131. Applicants submit that the applied art does not show each and every feature of the claimed invention.

Claims 1, 5, and 31-33

Independent claim 1 recites, in pertinent part, *locating a problem structure using a shapes-processing tool*. SU does not disclose this feature.

The Examiner asserts that SU discloses this feature at pages 702 and 704. More specifically, the Examiner contends "the problem structure are the spot defects" (Final Office Action, page 2). Applicants respectfully disagree.

Applicants respectfully submit the Examiner has a fundamental misunderstanding of the disclosure of SU. That is, the Examiner seems to be of the opinion, as evidenced by remarks throughout the Final Office Action, that SU discloses forming spot defects on a wafer, forming wires on a wafer, identifying where wires pass over spot defects, and then moving the wires away from the spot defects. This, however, is not what is disclosed by SU.

Instead, SU discloses a strategy for minimizing faults in which increased wire spacing is used to reduce defect sensitivity of manufactured wafers. This increased spacing is determined before manufacturing of the wafer to lessen the likelihood of a fault should a "spot defect" happen to occur during manufacturing. As disclosed by SU, spot defects occur during the manufacturing process and result in spots of extra or missing material on the wafer. Since spot defects occur during the manufacture of the wafer, there is no way to determine where a spot defect will occur. Accordingly, SU proposes increasing wire spacing during layout design (i.e., before manufacturing) to minimize the possible effects of any spot defects that later occur during manufacturing.

In view of this, the Examiner's assertion that SU discloses *locating a problem structure using a shapes-processing tool* is inaccurate. SU does not locate spot defects using a shapes processing tool. In fact, SU does not even locate spot defects (because spot defects necessarily

originate in the manufacturing process after SU's optimization has occurred). Instead, SU discloses an optimization strategy that is employed in the layout design stage (i.e., before manufacturing). At this stage, it is impossible to know where spot defects will occur. However, by increasing the spacing between wires, the sensitivity to any defects that do occur may be minimized. Therefore, SU does not disclose *locating a problem structure using a shapes-processing tool,* as recited in claim 1.

Claims 5 and 31-33 depend from allowable claim 1, and are allowable at least for the reasons described above with respect to claim 1. Moreover, these claims recite additional features that are not disclosed by SU.

For example, SU does not disclose the wider structure comprises a wider wire, as recited in claim 31. The Examiner asserts that the a spot defect may comprise material such as extra wiring material. Applicants respectfully disagree and note that SU makes no mention whatsoever that a spot defect comprises wire material. An anticipation rejection under 35 U.S.C. §102 requires that the applied art contain each and every feature of the claimed invention – not that an element of the applied art "may" comprise a claimed feature. SU simply does not disclose that the spot defect comprises wiring material, and it is improper for the Examiner to read this feature into SU.

Claims 11, 12, 13, 16

Independent claim 11 recites, in pertinent part, *determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer.* SU does not disclose this feature.

The Examiner asserts that SU discloses these features at pages 702 and 704 and the abstract. Particularly, the Examiner contends "the local modification is the spreading of wires

located over the spot defects, the dishing-prone structure is the structure that would leave the spots of missing material on the wafer" (Final Office Action, page 4). Applicants respectfully disagree.

As discussed above with respect to claim 1, Applicants respectfully submit that the Examiner is misconstruing the disclosure of SU. That is, the Examiner seems to be of the opinion that SU discloses identifying where wires pass over spot defects, and then moving the wires away from the spot defects. This, however, is not what is disclosed by SU.

Instead, SU discloses a strategy for minimizing faults caused by spot defects by increasing wire spacing to reduce defect sensitivity. Spot defects occur during the manufacturing process, resulting in spots of extra or missing material on the wafer. Since spot defects occur during the manufacture of the wafer, there is no way to determine where a spot defect will occur. In light of this, SU proposes increasing wire spacing during layout design (i.e., before manufacturing) to minimize the possible effects of any spot defects that occur during manufacturing.

SU does not disclose or suggest identifying wires that pass over spot defects, and then moving the wires, as the Examiner seems to suggest. This would be impossible, since the location of spot defects is not known in the layout design stage. Instead, SU discloses maximizing the spacing between wires during the layout design stage so that, if any spot defects do occur later during manufacturing, such spot defects will not cause faults.

As such, SU does not disclose *determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer.* In fact, SU does not even disclose a pair of wires that pass over a structure of another layer, much less the step of determining such an occurrence. Moreover, the Examiner's assertion that "the local

modification is the spreading of wires located over the spot defects, the dishing-prone structure is the structure that would leave the spots of missing material on the wafer" is inaccurate. SU simply does not disclose wires passing over spot defects, much less a step of determining whether wires pass over spot defects. This is because, in the layout design stage where SU's optimization takes place, it is unknown where any spot defect will actually occur.

Furthermore, the Examiner's explanation does not even address the language of the claimed invention. That is, claim 11 recites *determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer.* The Examiner's explanation refers to local modification (i.e., spreading) of wires. However, this does not address the recited determining feature. Put another way, the Examiner has not identified any portion of SU that discloses *determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer.* Therefore, the rejection of claim 11 is improper and should be withdrawn.

Claims 12, 13, and 16 depend from allowable claim 11, and are allowable at least for the reasons described above with respect to claim 11. Moreover, these claims recite additional features that are not disclosed by SU.

Claims 18, 19, 20, 23

Independent claim 18 recites, in pertinent part:

> forming a dishing-prone structure on a lower layer;
> forming two minimum-spaced wires over the dishing-prone structure on an upper layer;
> increasing a space between the two minimum-spaced wires in a region over the dishing-prone structure;

The Examiner asserts that SU discloses these features at pages 702 and 704 and the abstract. Particularly, the Examiner contends "the dishing prone structure is the structure

causing the missing material on the wafer" (Final Office Action, page 5). Applicants respectfully disagree.

As discussed above with respect to claim 11, Applicants respectfully submit that the Examiner has an incorrect understanding of SU. That is, SU discloses a layout design strategy that increases the spacing between wires so that spot defects (formed later during manufacturing) do not cause faults. SU's described optimization strategy does not (and cannot) know the location of any spot defects, because the spot defects occur later during the manufacturing process.

To this end, SU does not disclose forming a spot defect, then forming wires over the spot defect, and then increasing the spacing between the wires, as the Examiner seems to suggest. The Examiner's reading of SU is simply incorrect. Instead, SU discloses that during the layout design stage (before manufacturing) the wires are spaced apart (according to a local cost minimization function) to reduce sensitivity to any defects that may happen to occur later in the manufacturing stage. Therefore, SU does not disclose *forming a dishing-prone structure on a lower layer; forming two minimum-spaced wires over the dishing-prone structure on an upper layer; and increasing a space between the two minimum-spaced wires in a region over the dishing-prone structure*, as recited in claim 18.

Put another way, even assuming *arguendo* that a spot defect could constitute a dishing-prone structure, which Applicants do not concede, there is simply no disclosure in SU of forming wires over the spot defect and then increasing the spacing of the wires over the spot defect. This is because, in SU, the spacing of the wires is increased in the layout design stage before manufacturing (i.e., before spot defects are even created). Therefore, SU does not disclose *forming a dishing-prone structure on a lower layer; forming two minimum-spaced wires over the*

dishing-prone structure on an upper layer; and increasing a space between the two minimum-spaced wires in a region over the dishing-prone structure, as recited in claim 18.

Claims 19, 20, 23 depend from allowable claim 18, and are allowable at least for the reasons described above with respect to claim 18. Moreover, these claims recite additional features that are not disclosed by SU.

Claims 25-28

Applicants have cancelled claims 25-30 from further consideration in this application. therefore, the instant rejection of claims 25-28 is now moot. Applicants are not conceding in this application that those claims are not patentable over the art cited by the Examiner, as the present cancellations are only for facilitating expeditious prosecution of the allowable subject matter noted by the examiner. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications.

Accordingly, Applicants respectfully request that the §102 rejection of claims 1, 5, 11-13, 16, 18-20, 23, 25-28, and 31-33 be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,
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